Class-A or B amplifier with complementary MOS

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Abstract

This invention relates to an AB class amplifier of mutual complementary metal-semiconductor containing an adaptive shift circuit, a compensation capacitor and a pass of output transistors. The adaptive shift circuit is composed of a current mirror circuit, crystal diodes, a switch transistor and a current source transistor which is connected in series with the said crystal diode as the bias to drive the switch transistor. Providing a low enough linear zone resistor as the feedback, it can reduce the quality factor of the convolution inductance and to suppress the peak value gain and maintain the desired marginal gain.

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Claim

1, a complementary metal-oxide-semiconductor AB class amplifier characterized in, it has the accurate shift circuit in fitting a nature position, a building-out capacitor and an output transistor is right, with the output of receiving a differential amplifier circuit, and provide by this accurate shift circuit in fitting nature position and amplify required dc bias and direct current amplification, and behind the phase compensation of building-out capacitor, by this output transistor to drive output, wherein, should include by the accurate shift circuit in fitting nature position:

A current mirroring circuit is including gate continuous a NMOS electric crystal and the 2nd NMOS electric crystal;

A NMOS crystal diode, its gate links to each other with the drain;

A NMOS switching transistor, its source electrode are connected to the drain of the 2nd NMOS transistor of this current mirroring circuit, and the drain of a NMOS transistor of this current mirroring circuit and the source electrode of this NMOS crystal diode are connected to its drain, and the continuous department of floodgate drain of this NMOS crystal diode is then connected to its gate;

A PMOS input amplifier transistor, the drain of this NMOS crystal diode is connected to its drain; And

A PMOS current source transistor, the source electrode of this NMOS switching transistor is connected to its drain.

2, metal-oxide-semiconductor AB class amplifier according to claim 1 complementary characterized in, wherein should export the transistor and constitute PMOS transistor and the NMOS transistor that is linked to each other by the drain, and the gate of this PMOS input amplifier transistor is connected to the gate of this PMOS transistor, and its source electrode is connected in the voltage source, and the source electrode of this NMOS switching transistor is connected to the gate of this NMOS transistor, and the electronegative potential in the system is connected to its source

electrode.

3, metal-oxide-semiconductor AB class amplifier according to claim 2 complementary characterized in, wherein this building-out capacitor is connected between the gate of the drain of this PMOS transistor and this PMOS input amplifier transistor.

4, metal-oxide-semiconductor AB class amplifier according to claim 1 complementary characterized in, wherein the output of a differential amplifier circuit is connected to the gate of this PMOS input amplifier transistor, and the voltage source is then connected to its source electrode.

5, metal-oxide-semiconductor AB class amplifier according to claim 1 complementary characterized in, wherein bias voltage end is connected to the gate of this PMOS current source transistor, and the voltage source is then connected to its source electrode.

Claim

6, a complementary metal-oxide-semiconductor AB class amplifier characterized in, it has the accurate shift circuit in fitting a nature position, a building-out capacitor and an output transistor is right, with the output of receiving a differential amplifier, and provide by this accurate shift circuit in fitting nature position and amplify required dc bias and direct current amplification, and behind the phase compensation of building-out capacitor, by this output transistor to drive output, wherein, should include by the accurate shift circuit in fitting nature position:

A current mirroring circuit is including gate continuous a PMOS electric crystal and the 2nd PMOS electric crystal;

A PMOS crystal diode, its gate links to each other with the drain;

A PMOS switching transistor, its source electrode are connected to the drain of the 2nd PMOS transistor of this current mirroring circuit, and the drain of a PMOS transistor of this current mirroring circuit and the source electrode of this PMOS crystal diode are connected to its drain, and the continuous department of floodgate

drain of this PMOS crystal diode is then connected to its gate;

A NMOS input amplifier transistor, the drain of this PMOS crystal diode is connected to its drain; And

A NMOS current source transistor, the source electrode of this PMOS switching transistor is connected to its drain.

7, metal-oxide-semiconductor AB class amplifier according to claim 6 complementary characterized in, wherein should export the transistor and constitute NMOS transistor and the PMOS transistor that is linked to each other by the drain, and the gate of this NMOS input amplifier transistor is connected to the gate of this NMOS transistor, and the source electrode of this PMOS switching transistor is connected to the gate of this PMOS transistor.

8, the complementary metal-oxide-semiconductor AB class amplifier of claim 7 characterized in, wherein this building-out capacitor is connected between the gate of the drain of this NMOS transistor and this NMOS input amplifier transistor.

9, metal-oxide-semiconductor AB class amplifier according to claim 6 complementary characterized in, wherein the output of a differential amplifier circuit is connected to the gate of this NMOS input amplifier transistor, and system's electronegative potential is then connected to its source electrode.

10, metal-oxide-semiconductor AB class amplifier according to claim 6 complementary characterized in, wherein bias voltage end is connected to the gate of this NMOS current source transistor, and system's electronegative potential is then connected to its source electrode.

Complementary metal-oxide-semiconductor AB class amplifier

The invention relates to the technical field of amplifier circuit, especially indicate a complementary metal-oxide-

semiconductor AB class amplifier.

Known AB class amplifier is as illustrated in FIG. 4, mainly includes an input utmost point that comprises differential amplifier 41, and an output stage that comprises AB class amplifier 42, amplifies and the output of drive back in order to move the input signal difference of longitude.

Aforementioned AB class amplifier 42 can the small-signal analysis as follows:

With C_LIt is to put the open circuit voltage gain order to 0 for this AB class amplifier 42 of load capacitance by A:▒Wherein, r_B= r_{DS4}/ r_{DS5}For the direct current resistance (dcresistance) on the B point, r_O= r_{DS2}/ r_{DS6}For the direct current output resistance (dcoutput resistance) of output stage, gm_jRepresent the MOS transistor (Mj, j=1,2,3 ...) the parasitic capacitance (parasitic capacitance) that transfers electric field (transfreconductance), the current mirror amplifier that crystal M4, M5 constitute.

When providing a building-out capacitor C to aforementioned AB class amplifier 42_FWhen applying to in the operational amplifier circuit, it has building-out capacitor C_FOutput impedance be:▒Wherein, r_AThe direct current resistance of ordering for A, that is be the output resistance of differential amplifier, if $\omega > 1/(r_A C_F)$, just▒, then can derive:▒

Here,▒Represent an inductance that circles round output, wherein, $L_{OEQ} \approx C_B/(gm_1 gm_6)$, (4) and its have equivalent series resistance a: R_{SEQ}1/ (gm of $\approx_1 gm_6 r_B$), (5) consequently must:▒And because $gm_1 gm_6 r_B'' gm_2$, z_o(S), will resonate in following condition:▒ ▒And the resonant resistance below having:▒If and▒, then:▒If and $gm_2 r_B C_B > C_L$, then:▒

Can know by above analysis, because the building-out capacitor C of operational $amplifier_F$Can cause (gyration) the effect of circling round, and with inside stray capacitance C_B= C_{DB4}+ C_{DB5}+ C_{GD4}+ C_{GD5}+ $gm_6 r_O C_{GD6}$Circle round into the inductance in the output impedance, result in the output impedance of should resonating $|z_{OH}(j\omega_R)|$ will respond to and a peak gain counting the frequency department of MHz

to tens of MHz, make that the gain margin (gainmargin) of operational amplifier is not enough to be become negatively even, and then cause serious problem such as vibration. General design is for avoiding this problem to take place, must be with the gain margin design of the differential amplifier of the input stage of operational amplifier very low, nevertheless so can lead to the fact the gain duration to become very low, and can the volume of causing the direct current offset (dcoffset) grow etc. the problem.

In the document, the open number 09-018253 of Japanese patent proposes an operational amplifier circuit, though it can reduce r in known patent$_B$The equivalent value lighten aforementioned problem, nevertheless can lead to the fact the problem that the output drive ability is not enough, and make the effect improved extremely limited. Consequently, real modified necessity of giving of aforementioned known operational amplifier circuit.

The purpose of the invention is providing a complementary metal-oxide-semiconductor AB class amplifier, with under the unneccessary circumstances of sacrificing the gain duration, reaches the performance of power saving and big driving force.

According to one of characteristic of the invention,Its said complementary metal-oxide-semiconductor AB class amplifier,It is right to have the accurate shift circuit in fitting a nature position, a building-out capacitor and an output transistor,With the output of receiving a differential amplifier circuit,And provide by this accurate shift circuit in fitting nature position and amplify required dc bias and direct current amplification,And behind the phase compensation of building-out capacitor,Export transistor by this and export the drive,Wherein,Should include by the accurate shift circuit in fitting nature position: a current mirroring circuit,Including gate continuous a NMOS electric crystal and the 2nd NMOS electric crystal; A NMOS crystal diode,Its gate links to each other with the drain; A NMOS switching transistor,Its source electrode is connected to the drain of the 2nd NMOS transistor of this current mirroring circuit,The drain of a NMOS transistor of its

this current mirroring circuit of drain connection and the source electrode of this NMOS crystal diode,The continuous department of floodgate drain of this NMOS crystal diode is then connected to its gate; A PMOS input amplifier transistor,The drain of this NMOS crystal diode is connected to its drain; And,A PMOS current source transistor,The source electrode of this NMOS switching transistor is connected to its drain.

This wherein said output transistor constitutes PMOS transistor and the NMOS transistor that is linked to each other by the drain, and the gate of this PMOS input amplifier transistor is connected to the gate of this PMOS transistor, and its source electrode is connected in the voltage source, and the source electrode of this NMOS switching transistor is connected to the gate of this NMOS transistor, and the electronegative potential in the system is connected to its source electrode;

Wherein said this building-out capacitor is connected between the gate of the drain of this PMOS transistor and this PMOS input amplifier transistor;

Wherein the output of a differential amplifier circuit is connected to the gate of this said PMOS input amplifier transistor, and the voltage source is then connected to its source electrode;

Wherein bias voltage end is connected to the gate of this said PMOS current source transistor, and the voltage source is then connected to its source electrode.

According to another characteristic of the invention,It is right that its said complementary metal-oxide-semiconductor AB class amplifier has the accurate shift circuit in fitting a nature position, a building-out capacitor and an output transistor,With the output of receiving a differential amplifier,And provide by this accurate shift circuit in fitting nature position and amplify required dc bias and direct current amplification,And behind the phase compensation of building-out capacitor,Export transistor by this and export the drive,Wherein,Should include by the accurate shift circuit in fitting nature position: a current mirroring

circuit, Including gate continuous a PMOS electric crystal and the 2nd PMOS electric crystal; A PMOS crystal diode, Its gate links to each other with the drain; A PMOS switching transistor, Its source electrode is connected to the drain of the 2nd PMOS transistor of this current mirroring circuit, The drain of a PMOS transistor of its this current mirroring circuit of drain connection and the source electrode of this PMOS crystal diode, The continuous department of floodgate drain of this PMOS crystal diode is then connected to its gate; A NMOS input amplifier transistor, The drain of this PMOS crystal diode is connected to its drain; And, A NMOS current source transistor, The source electrode of this PMOS switching transistor is connected to its drain.

This wherein said output transistor constitutes NMOS transistor and the PMOS transistor that is linked to each other by the drain, and the gate of this NMOS input amplifier transistor is connected to the gate of this NMOS transistor, and the source electrode of this PMOS switching transistor is connected to the gate of this PMOS transistor;

Wherein said this building-out capacitor is connected between the gate of the drain of this NMOS transistor and this NMOS input amplifier transistor;

Wherein the output of a differential amplifier circuit is connected to the gate of this said NMOS input amplifier transistor, and system's electronegative potential is then connected to its source electrode;

Wherein bias voltage end is connected to the gate of this said NMOS current source transistor, and system's electronegative potential is then connected to its source electrode.

Now do the elaboration with figure and embodiment to the invention, wherein:

Fig. 1 is the circuit diagram of an invention preferred embodiment,

Fig. 2 shows at load capacitance C_LThe phase curve of the invention during for 100pF and the comparison diagram of the phase

curve of knowledge amplifier,

Fig. 3 is the circuit diagram of another preferred embodiment of the invention,

Fig. 4 shows known AB class operational amplifier circuit diagram.

The explanation of preferred embodiment:

For trying to achieve the complementary metal-oxide-semiconductor AB class amplifier of the invention, at first, through the problem of analysing aforementioned known technique, if make C_BIt, then must ideal output impedance a: y in order to constrain the resonance phenomenon to become more and more the $zero_{OH\_Ideal}= 1/z_{OH\_Ideal}= gm_2+ gm_1gm_6r_B+ sC_L$(12), consequently, can derive the impedance variation as follows:▒ ▒Then can derive:▒If and $gm_2r_BC_B> C_L$, the biggest loss that then can obtain the marginal gains is:▒

It can know to refer to formula (14) and (15), and the method of idealization of suppression resonance gain is with C_BThe value subtract to zero, nevertheless under actual conditions, C_BThe value can not be for zero, and consequently, the pratical and feasible best approach is reducing r_BThe value. For reaching this purpose, please consult the complementary metal-oxide-semiconductor AB class amplifier circuit picture of the shown invention of Fig. 1, it moves 11, one building-out capacitor C in (Level shift) the circuit by fitting a nature position quasi-$phase_F$Reach an output transistor and to 12 components, receive the output that comes from a differential amplifier circuit 13, amplify required dc bias and the direct current amplification coaxial with differential input I/P in order to provide by this fitting nature position accurate shift circuit 11, behind building-out capacitor CF's phase compensation, export transistor to 12 drive outputs by this.

It is as illustrated in FIG. 1,Should fitting nature position accurate shift circuit 11 include one as the PMOS transistor M1 of input amplifier and a PMOS transistor M5 as the current source, as two NMOS transistor M3 of current mirror and M4, a NMOS transistor M8 and the NMOS transistor M7 as the diode as the change-over

switch,Wherein,Connect the output (A point) of differential amplifier circuit 13 as the transistor M1's of input amplifier gate,Connect in bias voltage end VB1 as the transistor M5's of current source gate,Two transistor M1 and M5's source electrode is then connect voltage source VDD,Transistor M7's drain and switching transistor M8's source electrode are then connected respectively to its drain.Gate as the transistor M3 of current mirror and M4 links to each other, and links to each other with M3's drain, and these transistors M1, M3, M4 and M5 are used for providing the dc bias and the direct current amplification of the accurate shift circuit generally known promptly.

NOTE - PAGES 6-7 NOT AVAILABLE IN MACHINE TRANSLATION SERVICE

Aforesaid formula (14), (15), (25) and (26) are referred to, the r of the AB class amplifier of the invention can be known$_{DS8}$For operating in the resistance of linearity region, the about 110K Ω of its resistance value, and the resistance r of AB class amplifier in the known technique$_{B}$For operating in the saturation region, its resistance is 1.2M Ω, because r_{DS}Far be lighter than r_{B}, consequently, the gain peak value in the AB of invention class amplifier can be suppressed effectively.

When the work of the AB of invention class amplifier under the large-signal,And when desiring to export big source play electric current (source current),The A of input puts and is drawn low (pulled low),So transistor M2 can export big source play electric current,And transistor M1 can the conduction ratio quiescent current big transient current pass through transistor M7 and M3,And because transistor M4 and M3 are the current mirrors,So transistor M4 also can switch on so big transient current,And the transient current that

transistor M4 can switch on can be greater than the bias current of stablizing that transistor M5 provided,So it is low that the B point can be drawn,Transistor M6 can be close to and closes (turned off),The amplifier went out the electric current with the source that B class mode output is big this moment,In this transient state,Though transistor M8 and M7 also are the connections of electric current mirror,Nevertheless because its gain far is lighter than transistor M4 than M3's gain,, transistor M7 does not influence drop-down that B orders so only can switching on micro- electric current,Consequently, can not limit the source output capacity of AB class amplifier.

In addition when invention work under the large-signal, and when desiring to switch on big inspiration electric current (sink current), the A point is drawn high (pulled high), so transistor M1 and M2's on state current becomes very little, so transistor M7, M8, M3 and M4's on state current also becomes very little, and is lighter than the bias current of stablizing that transistor M5 provided, so the B point can be drawn high to being close to voltage source VDD, transistor M6 can switch on the heavy current, consequently, the amplifier will channel into big inspiration electric current from the load end with B class mode.

Reference diagram 2 is shown, and it shows at load capacitance C_LThe phase curve (A) of the invention during for 100pF and the phase curve (B) of known amplifier, AB class amplifier that can the obvious invention is very effective to the suppression of resonance peak value.

Fig. 3 is another preferred embodiment of the invention, and it is by fitting a nature position 31, one building-out capacitor C of accurate shift circuit$_L$And an output transistor is shown as in the figure to 32 components, should the accurate shift circuit in fitting nature position 31 including respectively as two NMOS transistor M1 of input amplifier and current source and M5, as the PMOS transistor M8 and the PMOS transistor M7 as the diode of two PMOS transistor M3 of current mirror and M4, a change-over switch, wherein, as the output (A point) and the bias voltage end VB1 of input amplifying circuit 33, the electronegative potential VSS of system is then

connected to its source electrode, transistor M7's drain and transistor M8's source electrode are then connected respectively to its drain.Gate as the transistor M3 of current mirror and M4 links to each other, and links to each other with M3's drain.

This output transistor constitutes 12 NMOS transistor M2 and the PMOS transistor M6 that are linked to each other by the drain, and wherein, transistor M1's gate is connected to transistor M2's gate, and transistor M8's source electrode is then connected to transistor M6's gate. This building-out capacitor C_FConnect between transistor M2's drain and transistor M1's gate. Transistor M7 sets up between the transistor M3 of transistor M1's output and current mirror, controls transistor M8 in order to provide the dc bias, is shown as in the figure, and transistor M8's source electrode is connected to transistor M4's drain (B point), and its drain is connected to transistor M3's drain and transistor M7's source electrode (C point), and transistor M7's the continuous department of floodgate drain (a D point) is then connected to its gate.

Its different only lying in with previous embodiment of the circuit of aforementioned embodiment replaces PMOS, NMOS transistor respectively with NMOS, PMOS transistor, the working method of its circuit is then identical with previous embodiment, consequently, and the workflow of this embodiment of not reduplication detailed description.

Can know by above explanation, the invention by string go into transistor M7 as the bias voltage with driving transistors M8, and can provide enough linear zone resistance r who hangs down$_{DS8}$As the feedback, consequently reduce the Q value of inductance of circling round effectively, and suppress the emergence of peak gain effectively, and keep required marginal gains, and this transistor M7 and M8's joining and binding mode still enabled to export transistor M6 when the large-signal driving voltage does not receive the strangulation, still enable the amplifier with the work of AB class

mode, reach the performance of power saving and big driving force, and the unnecessary duration that gains of sacrificing.

What should pay attention to is that above-mentioned a great deal of embodiment is only given an example for the ease of the explanation invention, but not limits the invention.

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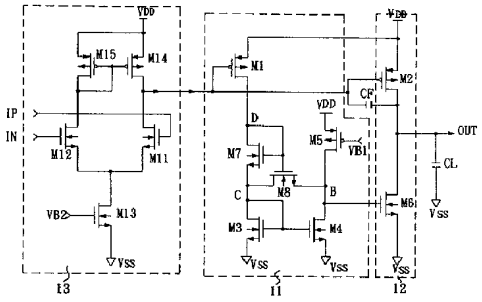
权利要求书2页 说明书9页 附图4页

[54]发明名称 互补式金氧半导体AB类放大器

[57]摘要

本发明为一种互补式金氧半导体AB类放大器，其包括一可适性位准位移电路、一补偿电容及一输出晶体管对，该可适性位准位移电路则由电流镜电路、晶体二极管、开关晶体管及电流源晶体管所构成，其由串入该晶体二极管以作为偏压来驱动开关晶体管，而提供一够低的线性区电阻作为反馈，故可降低回旋电感的Q值（品质因素）并有效地抑制峰值增益的发生，维持所需的边际增益。



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1、一种互补式金氧半导体 AB 类放大器，其特征在于，其具有一可适性位准位移电路、一补偿电容及一输出晶体管对，以接收一差动放大电路的输出，而由该可适性位准位移电路提供放大所需的直流偏压及直流放大作用，并经补偿电容的相位补偿后，由该输出晶体管对驱动输出，其中，该可适性位准位移电路包括：

一电流镜电路，包括闸极相连的第一 NMOS 电晶体及第二 NMOS 电晶体；

一 NMOS 晶体二极管，其闸极与汲极相连；

一 NMOS 开关晶体管，其源极连接至该电流镜电路的第二 NMOS 晶体管的汲极，其汲极连接该电流镜电路的第一 NMOS 晶体管的汲极与该 NMOS 晶体二极管的源极，其闸极则连接该 NMOS 晶体二极管的闸汲极相连处；

一 PMOS 输入放大器晶体管，其汲极连接该 NMOS 晶体二极管的汲极；以及

一 PMOS 电流源晶体管，其汲极连接该 NMOS 开关晶体管的源极。

2、如权利要求 1 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该输出晶体管对由汲极相连的 PMOS 晶体管及 NMOS 晶体管所构成，该 PMOS 晶体管的闸极连接该 PMOS 输入放大器晶体管的闸极，其源极连接于电压源，该 NMOS 晶体管的闸极连接该 NMOS 开关晶体管的源极，其源极连接于系统低电位。

3、如权利要求 2 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该补偿电容连接于该 PMOS 晶体管的汲极与该 PMOS 输入放大器晶体管的闸极之间。

4、如权利要求 1 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该 PMOS 输入放大器晶体管的闸极连接一差动放大电路的输出端，其源极则连接电压源。

5、如权利要求 1 所述的互补式金氧半导体 AB 类放大器，其特征在

于，其中该 PMOS 电流源晶体管的闸极连接一偏压端，其源极则连接电压源。

6、一种互补式金氧半导体 AB 类放大器，其特征在于，其具有一可适性位准位移电路、一补偿电容及一输出晶体管对，以接收一差动放大器的输出，而由该可适性位准位移电路提供放大所需的直流偏压及直流放大作用，并经补偿电容的相位补偿后，由该输出晶体管对驱动输出，其中，该可适性位准位移电路包括：

一电流镜电路，包括闸极相连的第一 PMOS 电晶体及第二 PMOS 电晶体；

一 PMOS 晶体二极管，其闸极与汲极相连；

一 PMOS 开关晶体管，其源极连接至该电流镜电路的第二 PMOS 晶体管的汲极，其汲极连接该电流镜电路的第一 PMOS 晶体管的汲极与该 PMOS 晶体二极管的源极，其闸极则连接该 PMOS 晶体二极管的闸汲极相连处；

一 NMOS 输入放大器晶体管，其汲极连接该 PMOS 晶体二极管的汲极；以及

一 NMOS 电流源晶体管，其汲极连接该 PMOS 开关晶体管的源极。

7、如权利要求 6 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该输出晶体管对由汲极相连的 NMOS 晶体管及 PMOS 晶体管所构成，该 NMOS 晶体管的闸极连接该 NMOS 输入放大器晶体管的闸极，该 PMOS 晶体管的闸极连接该 PMOS 开关晶体管的源极。

8、如权利要求 7 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该补偿电容连接于该 NMOS 晶体管的汲极与该 NMOS 输入放大器晶体管的闸极之间。

9、如权利要求 6 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该 NMOS 输入放大器晶体管的闸极连接一差动放大电路的输出端，其源极则连接系统低电位。

10、如权利要求 6 所述的互补式金氧半导体 AB 类放大器，其特征在于，其中该 NMOS 电流源晶体管的闸极连接一偏压端，其源极则连接系统低电位。

互补式金氧半导体 AB 类放大器

本发明是关于放大器电路的技术领域，尤其是指一种互补式金氧半导体 AB 类放大器。

公知的 AB 类放大器如图 4 所示，主要包括一由差动放大器 41 构成的输入极，以及一由 AB 类放大器 42 构成的输出级，以将输入信号经差动放大及驱动后输出。

前述 AB 类放大器 42 可以小信号分析如下：

以 C_L 为负载电容的该 AB 类放大器 42 由 A 点至 O 点的开路电压增益为：

$$A_{AO}(s)=\frac{V_O(s)}{V_A(s)}=(gm_2+gm_1gm_6\frac{r_B}{sC_Br_B+1})(\frac{r_O}{sC_Lr_O+1}) \quad (1)$$

其中，$r_B=r_{DS4}//r_{DS5}$ 为 B 点上的直流电阻（dcresistance），$r_O=r_{DS2}//r_{DS6}$ 为输出级的直流输出电阻（dcoutput resistance），gm_j 代表 MOS 晶体管（Mj，j=1，2，3…）的移转电场（transfreconductance），晶体 M4、M5 所构成的电流镜放大器的寄生电容（parasitic capacitance）。

当对前述 AB 类放大器 42 提供一补偿电容 C_F 以运用于运算放大器电路中时，其具有补偿电容 C_F 的输出阻抗为：

$$y_O(s)=1/z_O(s)=\frac{sC_Fr_A+1}{r_A}+\frac{sC_Fr_A}{sC_Fr_A+1}(gm_2+gm_1gm_6\frac{r_B}{sC_Br_B+1})+\frac{1}{r_O}+sC_L \quad (2)$$

其中，r_A 为 A 点的直流电阻，亦即为差动放大器的输出电阻，如果 $\omega>>1/(r_AC_F)$，且 $gm_2>>\frac{1}{r_A}+\frac{1}{r_O}$，则可导出：

$$y_{OH}(s) = 1/z_{OH}(s) = gm_2 + gm_1gm_6r_B\frac{1}{sC_Br_B+1} + sC_L \quad , \qquad (3)$$

在此，$gm_1gm_6r_B\frac{1}{sC_Br_B+1}$代表一回旋输出的电感，其中，

$$L_{OEQ} \approx C_B/(gm_1gm_6), \qquad (4)$$

且其具有一等效的串联电阻：

$$R_{SEQ} \approx 1/(gm_1gm_6r_B), \qquad (5)$$

因此可得：

$$z_{OH}(s) = \frac{sr_BC_B+1}{s^2r_BC_LC_B + sC_L + sgm_2r_BC_B + gm_1gm_6r_B + gm_2} \quad , \qquad (6)$$

而由于 $gm_1gm_6r_B \gg gm_2$， $z_O(S)$将共振于以下的条件：

$$\omega_R = \sqrt{\frac{gm_1gm_6r_B + gm_2}{r_BC_BC_L}} \approx \sqrt{\frac{1}{r_BC_B}}\sqrt{\frac{gm_1r_Bgm_6}{C_L}} = \sqrt{\frac{gm_1gm_6}{C_BC_L}} = \frac{1}{\sqrt{L_{OEQ}C_L}} \quad , \qquad (7)$$

$$Q_R = \frac{r_B}{C_L + gm_2r_BC_B}\sqrt{gm_1gm_6C_BC_L} = \frac{\sqrt{gm_2r_BC_BC_L}}{C_L + gm_2r_BC_B}\sqrt{\frac{gm_1r_Bgm_6}{gm_2}} \quad , \qquad (8)$$

并具有以下的共振阻抗：

$$|z_{OH}(j\omega_R)| = \left(\frac{1}{C_L + gm_2r_BC_B}\right)\sqrt{\frac{C_BC_L}{gm_1gm_6}}\sqrt{\frac{gm_1gm_6r_B^2C_B}{C_L} + 1} \quad , \qquad (9)$$

而如果 $\frac{gm_1gm_6r_B^2C_B}{C_L} \gg 1$，则：

$$|z_{OH}(j\omega_R)| \approx \frac{r_BC_B}{C_L + gm_2r_BC_B} \quad , \qquad (10)$$

且如果 $gm_2r_BC_B \gg C_L$，则：

$$|z_{OH}(j\omega_R)| \approx \frac{1}{gm_2} \quad 。 \qquad (11)$$

由以上分析可知，因为运算放大器的补偿电容 C_F 会引发回旋（gyration）作用，而将内部杂散电容 $C_B = C_{DB4} + C_{DB5} + C_{GD4} + C_{GD5} + gm_6r_OC_{GD6}$ 回旋成输出阻抗中的电感，导致该共振输出阻抗 $|z_{OH}(j\omega_R)|$ 在数 MHz 至

数十 MHz 的频率处将感应出一峰值增益，使得运算放大器的增益边际（gainmargin）不足甚至变成负的，进而引发振荡等严重的问题。一般的设计为避免此问题发生，必须将运算放大器的输入级的差动放大器的增益边际设计的很低，但如此却会造成增益频宽变得很低，且会引发直流偏移量（dcoffset）变大等问题。

在已知专利中文献中，日本专利公开号 09-018253 提出一种运算放大器电路，其虽然可以减少 r_B 的等效值来减轻前述问题，但却会造成输出驱动能力不足的问题，而使得改善的效果极其有限。因此，前述已知的运算放大器电路实有予以改进的必要。

本发明的目的在提供一种互补式金氧半导体 AB 类放大器，以在不必要牺牲增益频宽的情况下，达到省电及大驱动能力的性能。

依据本发明的特色之一，其所述的互补式金氧半导体 AB 类放大器，具有一可适性位准位移电路、一补偿电容及一输出晶体管对，以接收一差动放大电路的输出，而由该可适性位准位移电路提供放大所需的直流偏压及直流放大作用，并经补偿电容的相位补偿后，由该输出晶体管对驱动输出，其中，该可适性位准位移电路包括：一电流镜电路，包括闸极相连的第一 NMOS 电晶体及第二 NMOS 电晶体；一 NMOS 晶体二极管，其闸极与汲极相连；一 NMOS 开关晶体管，其源极连接至该电流镜电路的第二 NMOS 晶体管的汲极，其汲极连接该电流镜电路的第一 NMOS 晶体管的汲极与该 NMOS 晶体二极管的源极，其闸极则连接该 NMOS 晶体二极管的闸汲极相连处；一 PMOS 输入放大器晶体管，其汲极连接该 NMOS 晶体二极管的汲极；以及，一 PMOS 电流源晶体管，其汲极连接该 NMOS 开关晶体管的源极。

其中所述的该输出晶体管对由汲极相连的 PMOS 晶体管及 NMOS 晶体管所构成，该 PMOS 晶体管的闸极连接该 PMOS 输入放大器晶体管的闸极，其源极连接于电压源，该 NMOS 晶体管的闸极连接该 NMOS 开关晶体管的源极，其源极连接于系统低电位；

其中所述的该补偿电容连接于该 PMOS 晶体管的汲极与该 PMOS 输入放大器晶体管的闸极之间；

其中所述的该 PMOS 输入放大器晶体管的闸极连接一差动放大电路

的输出端，其源极则连接电压源；

其中所述的该 PMOS 电流源晶体管的闸极连接一偏压端，其源极则连接电压源。

依据本发明的另一特色，其所述的互补式金氧半导体 AB 类放大器具有一可适性位准位移电路、一补偿电容及一输出晶体管对，以接收一差动放大器的输出，而由该可适性位准位移电路提供放大所需的直流偏压及直流放大作用，并经补偿电容的相位补偿后，由该输出晶体管对驱动输出，其中，该可适性位准位移电路包括：一电流镜电路，包括闸极相连的第一 PMOS 电晶体及第二 PMOS 电晶体；一 PMOS 晶体二极管，其闸极与汲极相连；一 PMOS 开关晶体管，其源极连接至该电流镜电路的第二 PMOS 晶体管的汲极，其汲极连接该电流镜电路的第一 PMOS 晶体管的汲极与该 PMOS 晶体二极管的源极，其闸极则连接该 PMOS 晶体二极管的闸汲极相连处；一 NMOS 输入放大器晶体管，其汲极连接该 PMOS 晶体二极管的汲极；以及，一 NMOS 电流源晶体管，其汲极连接该 PMOS 开关晶体管的源极。

其中所述的该输出晶体管对由汲极相连的 NMOS 晶体管及 PMOS 晶体管所构成，该 NMOS 晶体管的闸极连接该 NMOS 输入放大器晶体管的闸极，该 PMOS 晶体管的闸极连接该 PMOS 开关晶体管的源极；

其中所述的该补偿电容连接于该 NMOS 晶体管的汲极与该 NMOS 输入放大器晶体管的闸极之间；

其中所述的该 NMOS 输入放大器晶体管的闸极连接一差动放大电路的输出端，其源极则连接系统低电位；

其中所述的该 NMOS 电流源晶体管的闸极连接一偏压端，其源极则连接系统低电位。

下面以附图和实施例对本发明作详细说明，其中：

图 1 为本发明一较佳实施例的电路图，

图 2 显示在负载电容 C_L 为 100pF 时本发明的相位曲线与知放大器的相位曲线的比较图，

图 3 为本发明另一较佳实施例的电路图，

图 4 显示已知的 AB 类运算放大器电路图。

较佳实施例说明：

为求得本发明互补式金氧半导体 AB 类放大器，首先，经分析前述已知技术的问题，如令 C_B 趋于零以压抑共振现象，则可得一理想的输出阻抗：

$$y_{OH\_Ideal} = 1/z_{OH\_Ideal} = gm_2 + gm_1 gm_6 r_B + sC_L \qquad (12)$$

因此，可导出阻抗变异如下：

$$z_{OH}(s)/z_{OH\_Ideal}(s) = \frac{(sC_L + gm_2 + gm_1 gm_6 r_B)(sr_B C_B + 1)}{s^2 r_B C_L C_B + sC_L + sgm_2 r_B C_B + gm_1 gm_6 r_B + gm_2}$$

$$= 1 + \frac{sgm_1 gm_6 r_B{}^2 C_B}{s^2 r_B C_L C_B + sC_L + sgm_2 r_B C_B + gm_1 gm_6 r_B + gm_2} \quad , \quad (13)$$

则可导出：

$$\frac{z_{OH}(j\omega_R)}{z_{OH\_Ideal}(j\omega_R)} = 1 + \frac{gm_1 gm_6 r_B{}^2 C_B}{C_L + gm_2 r_B C_B} \quad , \qquad (14)$$

且如果 $gm_2 r_B C_B >> C_L$，则可得到边际增益的最大损失为：

$$\frac{z_{OH}(j\omega_R)}{z_{OH\_Ideal}(j\omega_R)} = 1 + \frac{gm_1 gm_6 r_B}{gm_2} \approx \frac{gm_1 gm_6 r_B}{gm_2} \quad 。 \qquad (15)$$

参考公式（14）及（15）可知，压制共振增益的理想化方法乃将 C_B 的值减为零，但在实际情况下，C_B 值不可能为零，因此，实际可行的最佳方法乃在减少 r_B 的值。为达到此目的，请参照图 1 所示本发明的互补式金氧半导体 AB 类放大器电路图，其由一可适性位准位移（Level shift）电路 11、一补偿电容 C_F 及一输出晶体管对 12 所构成，接收来自一差动放大电路 13 的输出，以由该可适性位准位移电路 11 提供放大所需的直流偏压及与差动输入 I/P 同轴的直流放大作用，经补偿电容 CF 的相位补偿后，由该输出晶体管对 12 驱动输出。

如图 1 所示，该可适性位准位移电路 11 包括一作为输入放大器的 PMOS 晶体管 M1 及一作为电流源的 PMOS 晶体管 M5、作为电流镜的两 NMOS 晶体管 M3 及 M4、一作为切换开关的 NMOS 晶体管 M8 及一

作为二极管的 NMOS 晶体管 M7，其中，作为输入放大器的晶体管 M1 的闸极连接差动放大电路 13 的输出端（A 点），作为电流源的晶体管 M5 的闸极连接于一偏压端 VB1，而两晶体管 M1 及 M5 的源极则连接电压源 VDD，其汲极则分别连接晶体管 M7 的汲极及开关晶体管 M8 的源极。作为电流镜的晶体管 M3 及 M4 的闸极相连，并与 M3 的汲极相连，而此等晶体管 M1、M3、M4 及 M5 即用以提供一般所知的位准位移电路的直流偏压及直流放大作用。

该输出晶体管对 12 由汲极相连的 PMOS 晶体管 M2 及 NMOS 晶体管 M6 所构成，其中，晶体管 M2 的闸极连接晶体管 M1 的闸极，晶体管 M6 的闸极则连接晶体管 M8 的源极。该补偿电容 C_F 连接于晶体管 M2 的汲极与晶体管 M1 的闸极之间。

本发明由将晶体管 M7 设置于晶体管 M1 的输出及电流镜的晶体管 M3 之间，以提供直流偏压来控制晶体管 M8，如图所示，晶体管 M7 的闸极与汲极相连而形成一个二极管，晶体管 M8 的源极连接至晶体管 M4 的汲极（B 点），其汲极连接至晶体管 M3 的汲极与晶体管 M7 的源极（C 点），其闸极则连接晶体管 M7 的闸汲极相连处（D 点）。

当本发明的 AB 类放大器工作于小信号时，晶体管 M8 的汲源极电压 Vds 相当小，亦即晶体管 M8 工作于线性区（linear region，或称为 triode region），故具有相当小的汲源极电阻 r_{DS7}，因此可求得 AB 类放大器的输出阻抗为：

$$y_O(s) = 1/z_O(s) = \frac{sC_F r_A + 1}{r_A} + \frac{sC_F r_A}{sC_F r_A + 1}\left(gm_2 + \frac{1}{2} gm_1 gm_6 \frac{r_{DS8}}{sC_B r_{DS8} + 1}\right) + \frac{1}{r_O} + sC_L \quad , \tag{16}$$

其中，$C_B = C_{GD8} + C_{DB8} + C_{DB4} + C_{DB5} + C_{GD4} + C_{GD5} + gm_6 r_O C_{GD6}$，其将回旋出一输出电感：

$$L_{OEQ} \approx 2C_B/(gm_1 gm_6) \quad , \tag{17}$$

此电感具有一等效串联电阻：

$$R_{SEQ} = 2/(gm_1 gm_6 r_{DS8}) \quad , \tag{18}$$

而如果 $\omega >> 1/(r_A C_F)$ 且 $gm_2 >> \frac{1}{r_A} + \frac{1}{r_O}$ 则可简化为：

$$z_O(s) = \frac{(sC_B r_{DS8} + 1)/gm_2}{s^2 C_L C_B r_{DS8}/gm_2 + sC_L/gm_2 + sC_B r_{DS8} + gm_1 gm_6 r_{DS8}/2gm_2 + 1} \quad , \quad (19)$$

且如果 $gm_1 gm_6 r_{DS8}/2 >> gm_2$ ， 则输出阻抗具有一共振频率：

$$\omega_R = \sqrt{\frac{gm_1 gm_6 r_{DS8}/2 + gm_2}{r_{DS8} C_B C_L}} \approx \sqrt{\frac{1}{r_{DS8} C_B}} \sqrt{\frac{gm_1 r_{DS8} gm_6/2}{C_L}} = \sqrt{\frac{gm_1 gm_6}{2C_B C_L}} = \frac{1}{\sqrt{L_{OEQ} C_L}} \quad , \quad (20)$$

$$Q_R = \frac{r_{DS8}}{C_L + gm_2 r_{DS8} C_B} \sqrt{\frac{gm_1 gm_6 C_B C_L}{2}} \quad , \quad (21)$$

及一共振阻抗：

$$|z_{OH}(j\omega_R)| = \left(\frac{1}{C_L + gm_2 r_{DS8} C_B}\right) \sqrt{\frac{2C_B C_L}{gm_1 gm_6}} \sqrt{\frac{gm_1 gm_6 r_{DS8}^2 C_B}{2C_L} + 1} \quad 。 \quad (22)$$

相较于理想状况（C_B 趋近于 0 以完全压抑共振现象）时的输出阻抗：

$$y_{OH\_Ideal} = 1/z_{OH\_Ideal} = gm_2 + gm_1 gm_6 r_B + sC_L \quad , \quad (23)$$

可导出如下的阻抗变异：

$$z_{OH}(s)/z_{OH\_Ideal}(s) = 1 + \frac{sgm_1 gm_6 r_{DS8}^2 C_B/2}{s^2 r_{DS8} C_L C_B + sC_L + sgm_2 r_{DS8} C_B + gm_1 gm_6 r_{DS8}/2 + gm_2} \quad , \quad (24)$$

因此， $\frac{z_{OH}(j\omega_R)}{z_{OH\_Ideal}(j\omega_R)} = 1 + \frac{1}{2} \frac{gm_1 gm_6 r_{DS8}^2 C_B}{C_L + gm_2 r_{DS8} C_B}$ ， (25)

而如果 $gm_2 r_{DS8} C_B >> C_L$ ，即可得到增益边际（gain margin）的最大损失：

$$\frac{z_{OH}(j\omega_R)}{z_{OH\_Ideal}(j\omega_R)} = 1 + \frac{gm_1 gm_6 r_{DS8}}{2gm_2} \approx \frac{gm_1 gm_6 r_{DS8}}{2gm_2} \qquad (26)$$

参考前述的公式（14）、（15）、（25）及（26），可知本发明的 AB 类放大器的 r_{DS8} 为操作于线性区域的电阻，其阻抗值约 110KΩ，而已知技术中 AB 类放大器的电阻 r_B 为操作于饱和区，其阻值为 1.2MΩ，由于 r_{DS} 远小于 r_B，因此，于本发明的 AB 类放大器中的增益峰值将可有效地予以压制。

当本发明的 AB 类放大器工作于大信号下，且欲输出大的源出电流（source current）时，输入端的 A 点被拉低（pulled low），所以晶体管 M2 会输出大的源出电流，而晶体管 M1 会导通比静态电流大的暂态电流通过晶体管 M7 及 M3，且由于晶体管 M4 及 M3 是电流镜，所以晶体管 M4 也可以导通如此大的暂态电流，而晶体管 M4 可以导通的暂态电流会大于晶体管 M5 所提供的稳定偏压电流，所以 B 点会被拉低，晶体管 M6 会接近关闭（turned off），此时放大器以 B 类模式输出大的源出电流，在此暂态中，晶体管 M8 与 M7 虽然也是电流镜式的联结，但因为它的增益远小于晶体管 M4 比 M3 的增益，所以晶体管 M7 仅会导通微量电流而不影响 B 点的下拉，因此不会限制 AB 类放大器的源出能力。

另当本发明工作在大信号下，而欲导通大的汲入电流（sink current）时，A 点被拉高（pulled high），所以晶体管 M1 及 M2 的导通电流变得很小，因此晶体管 M7、M8、M3 与 M4 的导通电流也变得很小，且小于晶体管 M5 所提供的稳定偏压电流，所以 B 点会被拉高至接近电压源 VDD，晶体管 M6 可以导通大电流，因此，放大器将以 B 类模式自负载端导入大的汲入电流。

参考图 2 所示，其显示在负载电容 C_L 为 100pF 时本发明的相位曲线（A）与已知放大器的相位曲线（B），可以显见本发明的 AB 类放大器对共振峰值的抑制非常有效。

图 3 为本发明的另一较佳实施例，其由一可适性位准位移电路 31、一补偿电容 C_L 及一输出晶体管对 32 所构成，如图所示，该可适性位准

位移电路 31 包括分别作为输入放大器与电流源的两 NMOS 晶体管 M1 及 M5、作为电流镜的两 PMOS 晶体管 M3 及 M4、一切换开关的 PMOS 晶体管 M8 及一作为二极管的 PMOS 晶体管 M7，其中，作为输入放大电路 33 的输出端(A 点)及一偏压端 VB1，其源极则连接系统低电位 VSS，其汲极则分别连接晶体管 M7 的汲极及晶体管 M8 的源极。作为电流镜的晶体管 M3 及 M4 的闸极相连，并与 M3 的汲极相连。

该输出晶体管对 12 由汲极相连的 NMOS 晶体管 M2 及 PMOS 晶体管 M6 所构成，其中，晶体管 M2 的闸极连接晶体管 M1 的闸极，晶体管 M6 的闸极则连接晶体管 M8 的源极。该补偿电容 C_F 连接于晶体管 M2 的汲极与晶体管 M1 的闸极之间。晶体管 M7 设置于晶体管 M1 的输出及电流镜的晶体管 M3 之间，以提供直流偏压来控制晶体管 M8，如图所示，晶体管 M8 的源极连接至晶体管 M4 的汲极（B 点），其汲极连接至晶体管 M3 的汲极与晶体管 M7 的源极（C 点），其闸极则连接晶体管 M7 的闸汲极相连处（D 点）。

前述实施例的电路其与前一实施例的不同仅在于将 PMOS、NMOS 晶体管分别以 NMOS、PMOS 晶体管予以取代，其电路的工作方式则与前一实施例完全相同，因此，不再重复详述此实施例的工作流程。

由以上说明可知，本发明由串入晶体管 M7 作为偏压以驱动晶体管 M8，而得以提供一够低的线性区电阻 r_{DS8} 作为反馈，因此有效地降低回旋电感的 Q 值，并有效地抑制峰值增益的发生，而维持所需的边际增益，且此晶体管 M7 及 M8 的加入与连结方式在大信号时仍能使输出晶体管 M6 的驱动电压不受箝制，仍能使放大器以 AB 类模式工作，达到省电及大驱动能力的性能，且不必牺牲增益频宽。

应注意的是，上述诸多实施例仅为了便于说明本发明而举例而已，而非限制本发明。

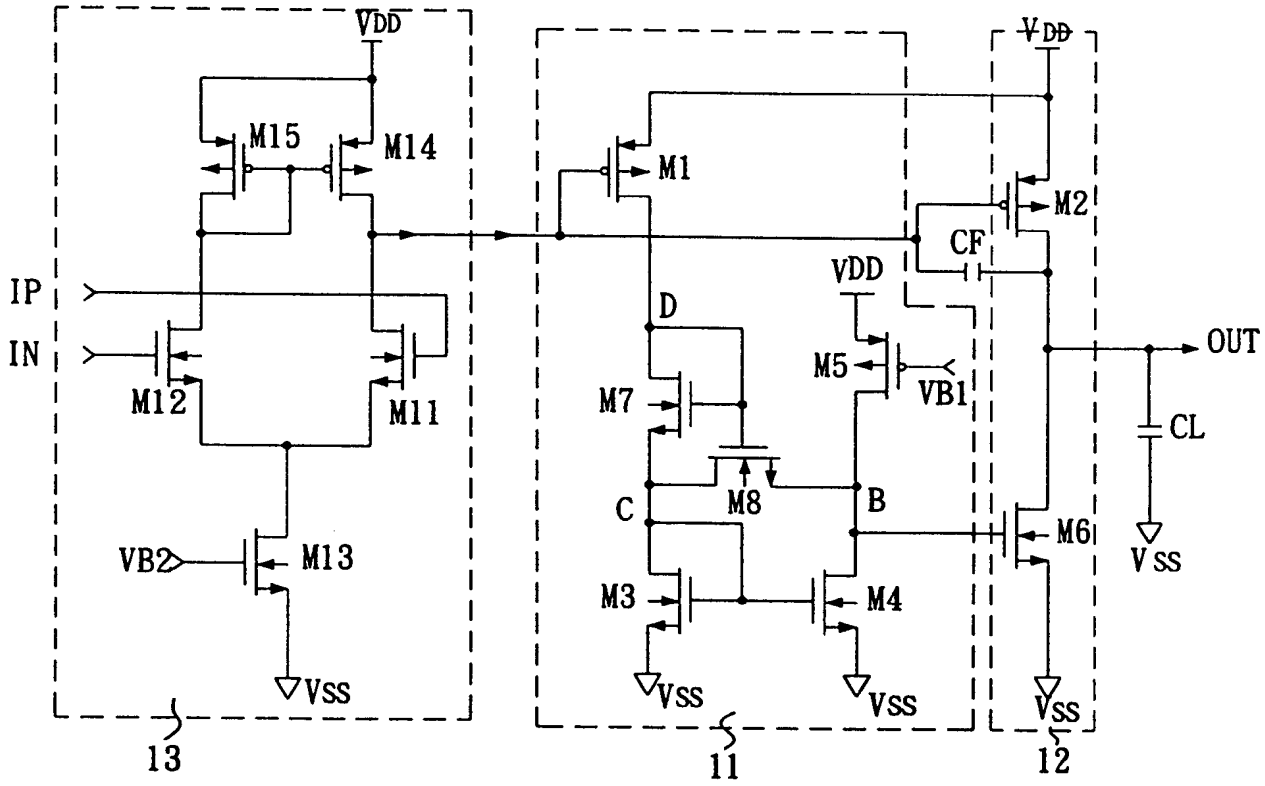
VDD
M15
M14
M1
M2
CF
IP
IN
M12
M11
D
M5
VB1
OUT
M7
CL
M8
C
B
VB2
M13
M6
VSS
M3
M4
VSS
VSS
VSS
VSS
13
11
12

图 1

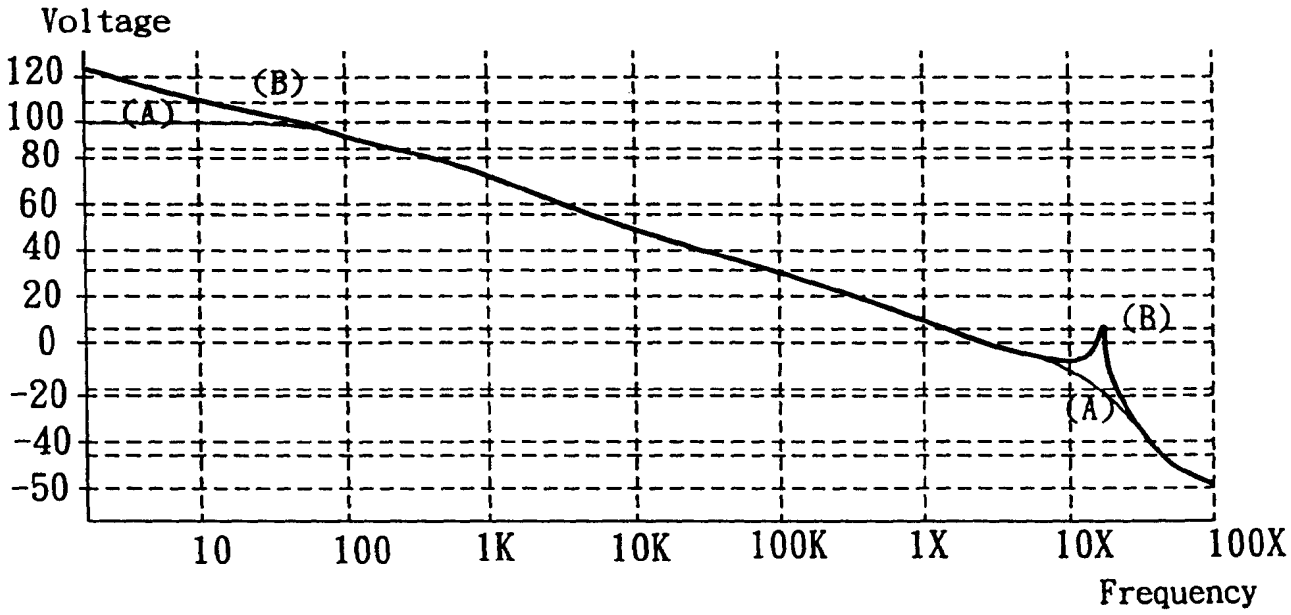
Voltage
120
100
80
60
40
20
0
-20
-40
-50
(B)
(A)
(B)
(A)
10
100
1K
10K
100K
1X
10X
100X
Frequency

图 2

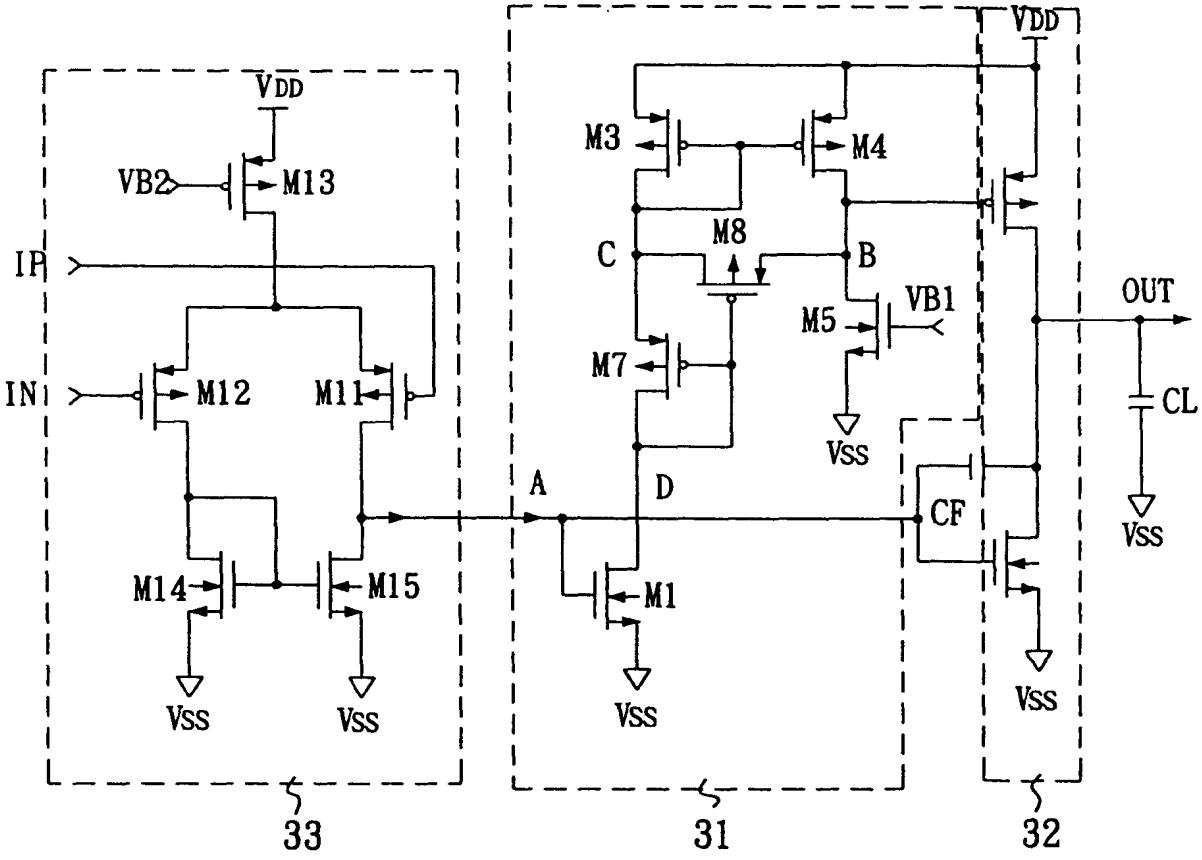
VDD
VB2
M13
IP
IN
M12
M11
M14
M15
Vss
Vss
33
M3
M4
C
M8
B
M5
VB1
M7
Vss
A
D
M1
Vss
31
VDD
CF
OUT
CL
Vss
Vss
32

图 3

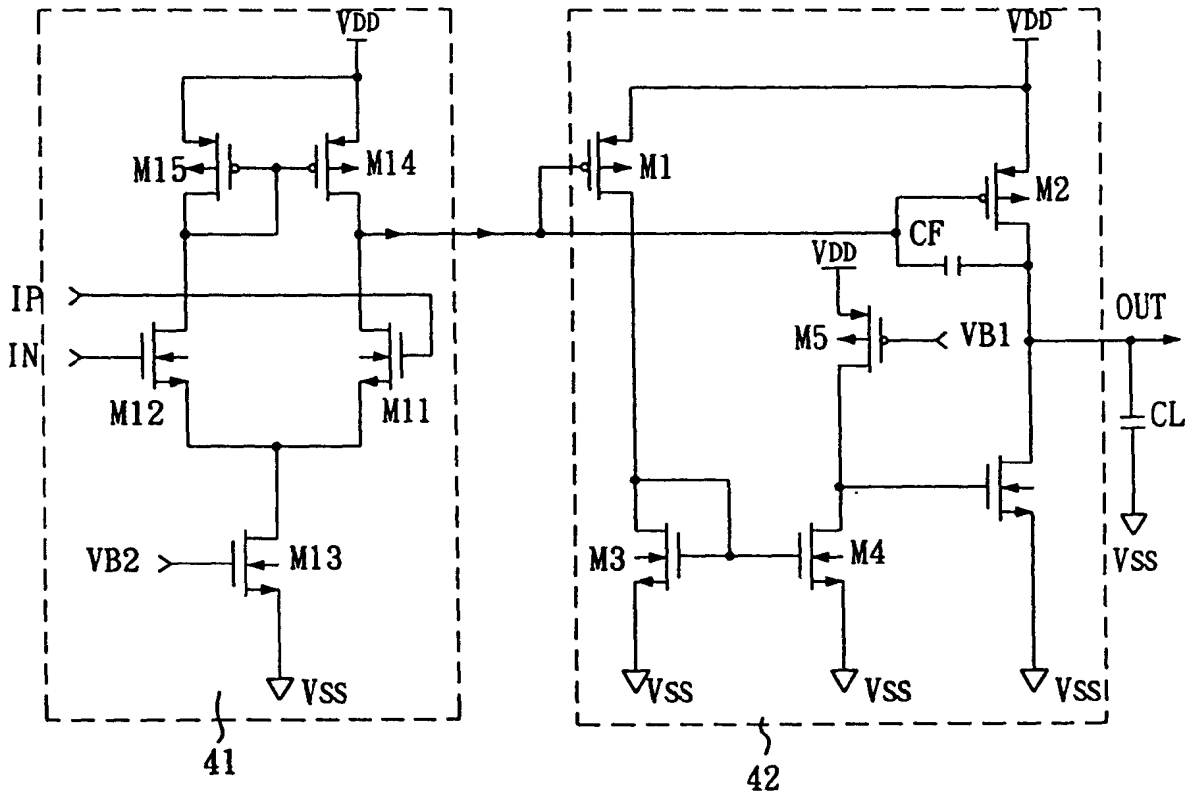
VDD
M15
M14
IP
IN
M12
M11
VB2
M13
Vss
41
VDD
M1
M2
CF
VDD
M5
VB1
OUT
CL
M3
M4
Vss
Vss
Vss
Vss
42

图 4